

**CLAIMS :**

Cancel the claims of record (1 to 20) and substitute new claims 21 to 30 as follows:

21. A mask-programmable read-only memory, comprising:
  - a first and a second address-selection lines, said first address-selection line crossing said second address-selection line;
  - a dielectric between said first and second address-selection lines;
  - a first memory cell comprising a first opening in said dielectric, said first opening being wider than a selected one of said first and second address-selection lines.
22. The mask-programmable read-only memory according to claim 21, further comprising:
  - a second memory cell adjacent to said first memory cell and comprising a second opening in said dielectric, said first and second openings being portions of a single opening.
23. The mask-programmable read-only memory according to claim 21, further comprising:
  - a second memory cell adjacent to said first memory cell and comprising a second opening in said dielectric, wherein said first and second openings are merged into a single opening.
24. The mask-programmable read-only memory according to claim 21, further comprising:
  - a third memory cell comprising no opening in said dielectric.
25. The mask-programmable read-only memory according to claim 21, wherein:
  - said first opening being wider than said first address-selection line; and
  - said first opening being wider than said second address-selection line.
26. A mask-programmable read-only memory, comprising:
  - a first and second address-selection lines, said first address-selection line crossing said second address-selection line;
  - a dielectric between said first and second address-selection lines;

a first memory cell having a first opening in said dielectric, the dimension of said first opening being larger than the dimension of said first address-selection line along the direction of said second address-selection line.

27. The mask-programmable read-only memory according to claim 26, further comprising:

a second memory cell adjacent to said first memory cell and comprising a second opening in said dielectric, said first and second openings being portions of a single opening.

28. The mask-programmable read-only memory according to claim 26, further comprising:

a second memory cell adjacent to said first memory cell and comprising a second opening in said dielectric, wherein said first and second openings are merged into a single opening.

29. The mask-programmable read-only memory according to claim 26, further comprising:

a third memory cell comprising no opening in said dielectric.

30. The mask-programmable read-only memory according to claim 26, wherein:

the dimension of said first opening being larger than the dimension of said second address-selection line along the direction of said first address-selection line.